AMENDMENTS TO THE CLAIMS

1-13. (Cancelled)

14. (New) A synchronization establishment apparatus operable to establish synchronization from a received signal that contains a synchronization establishment signal whose change in phase periodically alternates between positive and negative, said synchronization establishment apparatus comprising:

positive/negative change timing detection means for detecting a timing of changes in the positive/negative polarity of the change in phase of the synchronization establishment signal contained in the received signal;

synchronization establishment means for establishing synchronization from the received signal based on the timing detected by said positive/negative change timing detection means;

an A/D converter operable to convert the received signal from an analog signal to a digital signal;

a phase detection circuit operable to, based on the converted digital signal, demodulate I component data and Q component data, acquire the phase corresponding to the absolute value of the I component data and the absolute value of the Q component data, output a value which is the value of the acquired phase to which a negative polarity is applied when the positive/negative polarity of the I component data and the positive/negative polarity of the Q component data are different, and output a value which is the value of the acquired phase to which a positive polarity is applied when the positive/negative polarity of the I component data and the Q component data are the same;

an offset level generation circuit operable to generate and output an offset value which is equivalent to a phase rotation due to $\pi/4$-shift QPSK;

a first adder operable to add the value outputted from said phase detection circuit to the offset value outputted from said offset level generation circuit, and to output an added value;

an unwrap circuit operable to output an offset value that corrects discontinuity data when the phase has been rotated by π;

a second adder operable to add the added value outputted from said first adder to the offset value outputted from said unwrap circuit, and to output a second added value;

a filter circuit operable to filter the second added value outputted from said second adder and to outputs the filtered second added value;

a polarity bit converter operable to output data of different values when the polarity of the filtered second added value outputted from said filter circuit is positive than when the polarity of the filtered second added value is negative;

a change point extraction circuit operable to, based on the data outputted from said polarity bit converter, extract the positive/negative change points in the value of the waveform of the phase difference;

a change point measurement circuit operable to average the positive/negative change point timing of the phase difference extracted by said change point extraction circuit, and to output the averaged positive/negative change point timing;

a clock synchronization establishment circuit operable to, based on the averaged positive/negative change point timing outputted from said change point measurement circuit, establish clock synchronization; and

a timing generation circuit operable to, based on the timing at which the received signal starts, determine the position to reset a clock.

15. (New) A synchronization establishment apparatus according to claim 14, wherein synchronization is established for each received signal from a plurality of received signals.

16. (New) A synchronization establishment apparatus according to claim 14, wherein a preamble pattern in which 1001 is repeated in π /4-shift QPSK is used as the synchronization establishment signal, and a burst signal containing the preamble pattern is used as the received signal.

17. (New) A modem operable to modulate transmitted signals, to establish synchronization from a received signal that contains a synchronization establishment

signal whose change in phase periodically alternates between positive and negative, and to demodulate the received signal, said modem comprising:

modulating means for modulating transmitting signals;

positive/negative change timing detection means for detecting a timing of changes in the positive/negative polarity of the change in phase of the synchronization establishment signal contained in the received signal;

synchronization establishment means for establishing synchronization from the received signal based on the timing detected by said positive/negative change timing detection means;

demodulation means for demodulating the received signal according to the synchronization timing established by said synchronization establishment means;

an A/D converter operable to convert the received signal from an analog signal to a digital signal;

a phase detection circuit operable to, based on the converted digital signal, demodulate I component data and Q component data, acquire the phase corresponding to the absolute value of the I component data and the absolute value of the Q component data, output a value which is the value of the acquired phase to which a negative polarity is applied when the positive/negative polarity of the I component data and the positive/negative polarity of the Q component data are different, and output a value which is the value of the acquired phase to which a positive polarity is applied when the positive/negative polarity of the I component data and the Q component data are the same;

an offset level generation circuit operable to generate and output an offset value which is equivalent to a phase rotation due to $\pi/4$-shift QPSK;

a first adder operable to add the value outputted from said phase detection circuit to the offset value outputted from said offset level generation circuit, and to output an added value;

an unwrap circuit operable to output an offset value that corrects discontinuity data when the phase has been rotated by π;

a second adder operable to add the added value outputted from said first adder to the offset value outputted from said unwrap circuit, and to output a second added value;

a filter circuit operable to filter the second added value outputted from said second adder and to outputs the filtered second added value;

a polarity bit converter operable to output data of different values when the polarity of the filtered second added value outputted from said filter circuit is positive than when the polarity of the filtered second added value is negative;

a change point extraction circuit operable to, based on the data outputted from said polarity bit converter, extract the positive/negative change points in the value of the waveform of the phase difference;

a change point measurement circuit operable to average the positive/negative change point timing of the phase difference extracted by said change point extraction circuit, and to output the averaged positive/negative change point timing;

a clock synchronization establishment circuit operable to, based on the averaged positive/negative change point timing outputted from said change point measurement circuit, establish clock synchronization; and

a timing generation circuit operable to, based on the timing at which the received signal starts, determine the position to reset a clock.

18. (New) A modem according to claim 17, wherein synchronization is established for each received signal from a plurality of received signals, and each of the received signals is demodulated.

19. (New) A modem according to claim 17, wherein a preamble pattern in which 1001 is repeated in π /4-shift QPSK is used as the synchronization establishment signal, and a burst signal containing the preamble pattern is used as the received signal.

20. (New) A base station in a traffic information system in which base stations and mobile stations communicate wirelessly, said base station being operable to modulate signals and to wirelessly transmit the modulated signals to the mobile stations, to wirelessly receive a signal from the mobile stations that contains a synchronization establishment signal whose change in phase periodically alternates between positive and

negative, to establish synchronization from the received signal, and to demodulate the received signal, said base station comprising:

an antenna operable to transmit and receive wireless signals;

modulating means for modulating signals;

transmission means for wirelessly transmitting modulated signals to the mobile stations via said antenna;

receiving means for receiving, via said antenna, signals transmitted wirelessly from the mobile stations;

positive/negative change timing detection means for detecting a timing of changes in the positive/negative polarity of the change in phase of the synchronization establishment signal contained in the received signal;

synchronization establishment means for establishing synchronization from the received signal based on the timing detected by said positive/negative change timing detection means;

demodulation means for demodulating the received signal according to the synchronization timing established by said synchronization establishment means;

control means for communicating the signals exchanged with the mobile stations to an external apparatus;

an A/D converter operable to convert the received signal from an analog signal to a digital signal;

a phase detection circuit operable to, based on the converted digital signal, demodulate I component data and Q component data, acquire the phase corresponding to the absolute value of the I component data and the absolute value of the Q component data, output a value which is the value of the acquired phase to which a negative polarity is applied when the positive/negative polarity of the I component data and the positive/negative polarity of the Q component data are different, and output a value which is the value of the acquired phase to which a positive polarity is applied when the positive/negative polarity of the I component data and the Q component data are the same;

an offset level generation circuit operable to generate and output an offset value which is equivalent to a phase rotation due to $\pi/4$-shift QPSK;

a first adder operable to add the value outputted from said phase detection circuit to the offset value outputted from said offset level generation circuit, and to output an added value;

an unwrap circuit operable to output an offset value that corrects discontinuity data when the phase has been rotated by π;

a second adder operable to add the added value outputted from said first adder to the offset value outputted from said unwrap circuit, and to output a second added value;

a filter circuit operable to filter the second added value outputted from said second adder and to outputs the filtered second added value;

a polarity bit converter operable to output data of different values when the polarity of the filtered second added value outputted from said filter circuit is positive than when the polarity of the filtered second added value is negative;

a change point extraction circuit operable to, based on the data outputted from said polarity bit converter, extract the positive/negative change points in the value of the waveform of the phase difference;

a change point measurement circuit operable to average the positive/negative change point timing of the phase difference extracted by said change point extraction circuit, and to output the averaged positive/negative change point timing;

a clock synchronization establishment circuit operable to, based on the averaged positive/negative change point timing outputted from said change point measurement circuit, establish clock synchronization; and

a timing generation circuit operable to, based on the timing at which the received signal starts, determine the position to reset a clock.

21. (New) A base station according to claim 20, wherein synchronization is established for each received signal from a plurality of received signals, and each of the received signals is demodulated.

22. A base station according to claim 20, wherein a preamble pattern in which 1001 is repeated in π /4-shift QPSK is used as the synchronization establishment signal, and a

burst signal containing the preamble pattern is used as the received signal.